REMARKS

Present Status of Application

The Examiner is thanked for his continued indication that claims 3-7, 10-14, and 17-20 are allowable. The Office Action, however, rejected claims 1, 2, 8, 9, 15, and 16 under 35 U.S.C. § 103(a) as allegedly unpatentable over Provisional Application no. 60/093,830, filed on July 22, 1998, or U.S. Patent 6,499,129 B1 to Srinivasan et al. Claims 1, 8, and 15 are independent claims, while claims 2, 9, and 16 are dependent. Applicant respectfully traverses the rejections and requests reconsideration and withdrawal of all rejected claims.

Summary of Present Application

The present application is directed to a method and apparatus for evaluating a gate of an integrated circuit to determine whether or not the gate has acceptable immunity to noise. The apparatus comprises a computer configured to execute a rules checker program, which receives input relating to characteristics of a static gate contained in the integrated circuit. The gate comprises at least two field-effect transistors (FETs). Each FET has a width and the characteristics received in the input to the rules checker program include the widths of the field effect transistors. The rules checker program analyzes the widths of the FETs to determine whether or not the gate has an acceptable level of noise immunity.

Each gate typically comprises a plurality of FETs, usually an NFET and a PFET, and input terminals for receiving input signals. The rules checker program processes the widths of the PFETs and NFETs to obtain at least a first numerical value relating to the widths. The rules checker program utilizes the first numerical value to access one or more threshold noise-level values from a memory device in communication with the computer. The rules checker program determines noise levels on the inputs, either through calculation or simulation. The

rules checker program compares the determined noise levels with the threshold values and uses the results of the comparison to determine whether or not the gate has an acceptable immunity to noise.

Discussion of Office Action Rejections

Applicant respectfully traverses the rejections and submits that they should be withdrawn for separate and independent reasons. As more fully detailed below, Srinavasan is not prior art to the present application. Further, and more significantly, there are significant substantive distinctions between the Applicant's claimed invention and Srinavasan, as applied by the Office Action.

Srinivasan is NOT Prior Art to Applicant's Invention

The Office Action rejected claims of the present application as allegedly unpatentable over Provisional Application no. 60/093,830, filed on July 22, 1998, or U.S. Patent 6,499,129 B1 to Srinivasan et al. As Applicant has stated in a previous response, the issue patent cannot form the basis of a proper rejection, since the present application was filed before the filing date of that application. Therefore, any rejection of the presently-pending claims must be based on the provisional application. Indeed, all presently-outstanding rejections cite only teachings of the provisional application. Therefore, the issued patent ('129 patent) should be withdrawn from consideration.

With regard to the provisional application, Srinivasan is not prior art to the invention of the present application, and all rejections base on Srinivasan should be removed for at least this reason. Srinivasan claims the priority benefit of a provisional application that was filed on July 22, 1998 (a copy of which has been provided by the Examiner with the present Office Action.

However, the present invention was both conceived and reduced to practice prior to the filing date of the provisional application to which Srinavasan claims priority. In this regard, and to facilitate the prosecution of this application, the Applicant has attached (Tab A) an internal "Invention Disclosure" document, which documented the conception and reduction to practice of this invention. Certain portions of this document (not substantively related to the subject matter of this application) have been redacted for reasons of confidentiality. As shown on the first page of this document, this document was prepared and submitted (internally) to Hewlett-Packard Company on May 8, 1998 (BEFORE the filing date of the Srinivasan provisional application). Broadly, the Invention Disclosure of Tab A identifies one embodiment or implementation as:

> A method for determining the noise immunity of static gates which includes modeling the static gate as inverters and comparing voltage noise limits from the resulting inverters. The model inverters should be derived from the output strength of the gate.

(Tab A, p.2). Further, this document indicates that the implementation was built or tested (e.g., reduced to practice) in January 1997. This documentation clearly demonstrates that the subject matter of the present invention pre-dates the Srinivasan provisional filing, and therefore Srinivasan is not prior art to the claims of the present application.

The Applicant has not submitted a formal 131 declaration to accompany this response, as such is not believed to be necessary based in part upon the substantive distinctions set out below. Should, however, the Examiner maintain his reliance upon Srinavasan, and mail a subsequent Office Action that provides a copy of the provisional application (with the requisite support for a proper rejection), then Applicant may respond with a formal 131 declaration at that time.

For at least the foregoing reasons, Applicant respectfully requests that the rejection be withdrawn and all claims passed to issuance.

Substantive Distinctions of the Srinivasan Patent

Turning now to the specific rejections, the Office Action rejected claims 1, 2, 8, 9, 15, and 16 under 35 U.S.C. § 103(a), as allegedly unpatentable over Provisional Application no. 60/093,830. Applicant respectfully traverses this rejection for at least the reasons that follow.

Turning first to independent claim 1, independent claim 1 recites:

> 1. An apparatus ***for evaluating a gate to determine whether or not the gate has an acceptable immunity to noise***, the apparatus comprising:
> a computer configured to execute a rules checker program, the rules checker program receiving input relating to characteristics of a static gate contained in the integrated circuit, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors, ***the rules checker program analyzing the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity***.

Likewise, claim 15 recites:

> 15. A computer-readable medium containing a rules checker computer program, the computer program ***evaluating a gate to determine whether or not the gate has an acceptable immunity to noise***, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors, the program comprising:
> ***code which analyzes the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity.***

(*Emphasis added.*) Applicant respectfully traverses the rejection of independent claims 1 and 15 for at least the reason that Srinivasan fails to disclose or teach at least the features emphasized above.

Srinivasan is directed to a system and method for estimating or verifiying the ***performance*** of integrated circuit designs. Significantly, the Office Action does not even specifically allege that Srinivasan teaches the features emphasized above. Instead, the Office

Action only generally alleges that Srinivasan renders the claimed invention obvious, insofar as Srinivasan is allegedly directed to a

> ... method and system for estimating design performances, including handling cross-coupling effects, simultaneous switching, etc. for device characterization including noise analysis or noise immunity with feature limitations identical to the claims (Summary of the Invention, page 5, lines 18-26, for example)... [The] design rule checking includes a computer configured to execute a rule checker program (page 5, lines 18-26), wherein the design rule being checked for an integrated circuit design having gates, gate connected in datapath or along circuit paths including static gate characteristics, transistor parameters such as transistor widths, lengths, connected in device channel, etc. ("Summary of the Invention", pages 5 and 6, for instance). The design rule checker program is to check transistor performance such as timing, cross-talk due to wire coupling, switching delay (pages 5, 6, 7, 8, for example).

(Office Action, paragraph spanning pages 2 and 3). Significantly, the Office Action admits that Srinivasan does NOT teach the checking of noise immunity, and instead the Office Action merely subjectively alleges that:

> Practitioners in the art ... would have found Srinivasan disclosure of checking circuit performance above would ***imply*** the claimed step for checking noise immunity because Srinivasan rule checker program is for verification of tight coupling wires in gate channel connected components (pages 5-8), for example, and it would be known in the art such tightly coupling channel connected components would contribute to noise, switching delay in order to verify noise immunity.

(Office Action, page 3). Applicant respectfully submits that this rejection embodies fundamental misapplications of the teachings of Srinivasan.

First, by stating that the "Srinivasan disclosure ... would imply the claimed step for checking noise immunity," the Office Action effectively argues that this teaching is inherent in the Srinivasan. Applicant respectfully disagrees. The Federal Circuit has clearly-established precedence to this legal concept. To this end, the undersigned respectfully directs the Examiner's attention to the decision of *Elan Pharms. v. Mayo Found. for Med. Educ. & Research*, 304 F.3d 1221 (Fed. Cir. 2002), in which the Federal Circuit reversed a finding of

inherency by a district court. In this opinion, the Court of Appeals for the Federal Circuit emphasized:

> An anticipating reference "must disclose every element of the challenged claim and enable one skilled in the art to make the anticipating subject matter." *PPG Industries, Inc. v. Guardian Industries Corp.*, 75 F.3d 1558, 1566, 37 USPQ2d 1618, 1624 (Fed. Cir. 1996). When [a rejection] is based on inherency of limitations not expressly disclosed in the assertedly anticipating reference, it must be shown that the undisclosed information was known to be present in the subject matter of the reference. *Continental Can Co. USA, Inc. v. Monsanto Co.*, 948 F.2d 1264, 1269, 20 USPQ2d 1746, 1749-50 (Fed. Cir. 1991). ***An inherent limitation is one that is necessarily present; invalidation based on inherency is not established by "probabilities or possibilities."*** *Scaltech, Inc. v. Retec/Tetra, LLC.*, 178 F.3d 1378, 1384, 51 USPQ2d 1055, 1059 (Fed. Cir. 1999).

(*Emphasis added.*)

This discussion by the Federal Circuit is certainly nothing new. The law surrounding the doctrine of inherency has not changed for over 60 years. In fact, the Federal Circuit has repeatedly quoted the language from the 1939 decision *Hansgirg v. Kemmer*, 26 C.C.P.A. 937, 102 F.2d 212, 214, 40 U.S.P.Q. (BNA) 665, 667 (CCPA 1939)), which stated "Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing *may* result from a given set of circumstances is not sufficient."

The Manual of Patent Examining Procedure (MPEP) also embodies these requirements. Specifically, MPEP 2112, in part, states:

> The fact that a certain result or characteristic ***may*** occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic.... To establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in they thing described in that reference, and that it would be so recognized by persons of ordinary skill.

(*Emphasis in original*).

In contrast to these legal and procedural requirements, the Office Action has, unfortunately, substituted its own subjective judgment in place of the actual teachings of the

Srinivasan, in a manner that embodies clear (and improper) hindsight. In this regard, the Office Action has stated only that the claimed feature of noise immunity verification is implied in Srinivasan because the "Srinivasan rule checker program is for verification of tight coupling wires in gate channel connected components." This is clearly a situation where, at best, such a teaching that may be consistent with the other teachings of Srinivasan, but is certainly not necessarily present. Such situations are specifically addressed in the MPEP and Federal Circuit precedent, and do not constitute proper teachings for supporting a rejection of the claimed subject matter.

Further, the undersigned performed an electronic search of the entire text of the specification and claims of the issued Srinivasan patent, which search confirmed that the term "noise" is not used anywhere in the claims or specification of Srinivasan. Therefore, the allegation by the Office Action that Srinivasan teaches a system or method to check for the susceptibility of ***noise*** immunity is simply and clearly misplaced.

Consequently, and for at least these reasons, the rejection of independent claims 1 and 15 is deficient, and should be withdrawn. Should the Examiner maintain these rejections, a further Office Action is required, which provides more concrete and identifiable teachings to support this subjective allegation.

Further, and as a separate and independent basis for the patentability of claims 1 and 15, claim 1 specifies the ***analysis of widths of field effect transistors within a static gate***, to determine whether the gate has an acceptable ***noise immunity*** (claim 15 includes similar features). Simply stated, Srinivasan does not teach this claimed aspect, and therefore cannot properly be used to reject claims 1 or 15. The Office Action alleges that this is taught in the "Summary of the Invention" and on pages 5 and 6 of the Srinivasan provisional application. It is not. The undersigned has closely reviewed these portions of the Srinivasan provisional

application and has found absolutely no mention of nor reference to any analysis of transistor widths within a static gate in evaluating the design (much less in evaluating the noise immunity of the static gate, as required by claims 1 and 15). Should the Examiner disagree, the undersigned respectfully requests that the Examiner point to a specific teaching within this reference for these alleged teachings (and not just a general allegation, referencing multiple pages of the reference). For at least this additional reason, the rejection of claims 1 and 15 is misplaced and should be withdrawn.

Further, the Office Action repeatedly cites the "Summary of the Invention" and pages 5 and 6 of Srinivasan as allegedly teaching a number of aspects of the claimed invention. They do not. As can be verified from even a cursory review of these portions of Srinivasan, there is absolutely no teaching of significant features embodied in both independent claims 1 and 15, including: "evaluation of a gate to determine whether or not the gate has an acceptable immunity to noise" or "analyzing the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity." For at least these additional, and fundamental, shortcomings of Srinivasan, the rejections of independent claims 1 and 15 should be withdrawn.

For at least the foregoing reasons, Applicant respectfully submits that the rejection of claims 1 and 15 is misplaced and should be withdrawn. For at least these same reasons, claims 2 and 16, which depend from claims 1 and 15, respectively, patently define over Srinivasan as well.

Claims 8 and 9

The Office Action also rejected claims 8 and 9 under 35 U.S.C. § 102(e), as being anticipated by Srinivasan. Applicant respectfully traverses this rejection for at least the reasons that follow.

Independent claim 8 recites:

> 8. A method ***for evaluating a gate to determine whether or not the gate has an acceptable immunity to noise***, the method comprising the steps of:
>
> receiving input in a computer relating to characteristics of a static gate contained in the integrated circuit, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors; and
>
> ***analyzing the widths of the field effect transistors in the computer to determine whether or not the gate has an acceptable noise immunity, wherein the computer executes a rules checker program which analyzes the widths to determine whether or not the gate has an acceptable noise immunity.***

(*Emphasis added.*) Applicant respectfully traverses the rejection of claim 8 for at least the reason that Srinivasan fails to disclose or teach either of the features emphasized above.

The Office Action rejected claim 8, relying on the same portions of Srinivasan that the Office Action relied upon in rejecting claim 1. In this regard, the Office Action relied principally upon the "Summary of the Invention" and pages 5 and 6 of the Srinivasan provisional application (referenced above) and secondarily upon pages 7 and 8. Simply stated, and for the same reasons discussed in connection with claims 1 and 15 above, Srinivasan does NOT teach at least the features of claim 8 that are emphasized above (i.e., "evaluating a gate to determine whether or not the gate has an acceptable immunity to noise" or "analyzing the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity."

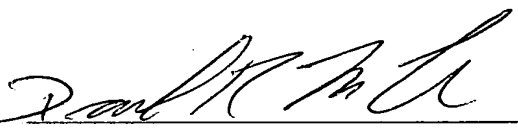
Consequently, and for the same reasons set forth in connection with claim 1, Applicant respectfully submits that the rejection of claims 8 is misplaced and should be withdrawn. For at least these same reasons, claim 9, which depends from claim 8, patently defines over Srinivasan as well.

CONCLUSION

In view of the foregoing, it is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

No fee is believed to be due in connection with this response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to Hewlett-Packard Company's deposit account No. 08-2025.

Respectfully submitted,

By: 

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